ICOS International Cooperation On Semiconductors

Challenges in Advanced Computing and Functionalities
International Cooperation on Semiconductors

Technology Highlights in Advanced Computing

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Presented by Ray Duffy (Tyndall National Institute, UCC)

SiNANO Institute

LV Annual Meeting of the Italian Society of Electronics
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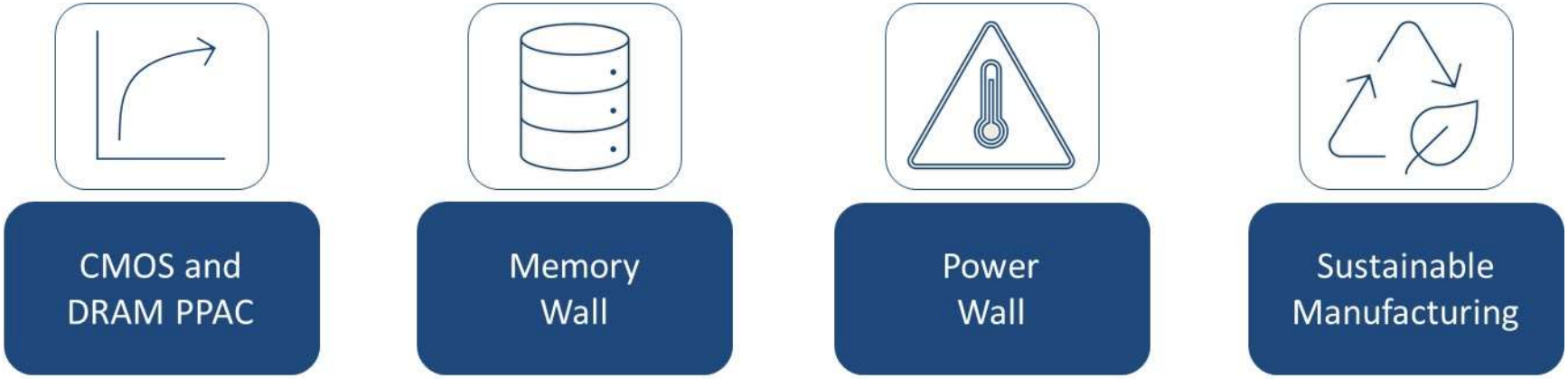
Outline

- Introduction: trends and challenges
- Computing roadmap:
  - CMOS device architecture
  - 2D materials for FEOL
  - New materials for BEOL
  - Lithography
  - CMOS 2.0
- Memory technologies
- Beyond Von Neumann disruptive approaches:
  - Near or in-memory computing
  - Quantum computing
- Heterogeneous integration: from chiplets to functional backside
- Analysis: EU and non-EU actors
- Conclusions

Summary

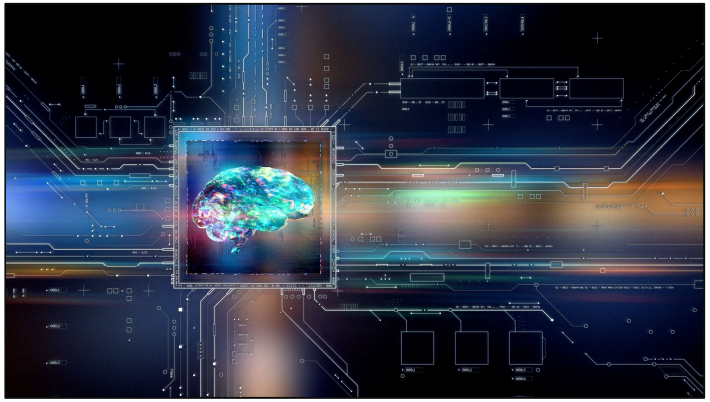
- Compute needs are growing at an unprecedented speed
- Innovations across different levels needed to enable chip & system performance enhancement
- Sustainability an increasingly important metric for evaluating technology choices
- Europe is very strong in R&D in all advanced compute areas



PPAC=Power-Performance-Area-Cost

Diversity of Applications and Workloads

GPUs for Training



High throughput parallel compute
Very high memory bandwidth
Very high GPU-GPU bandwidth

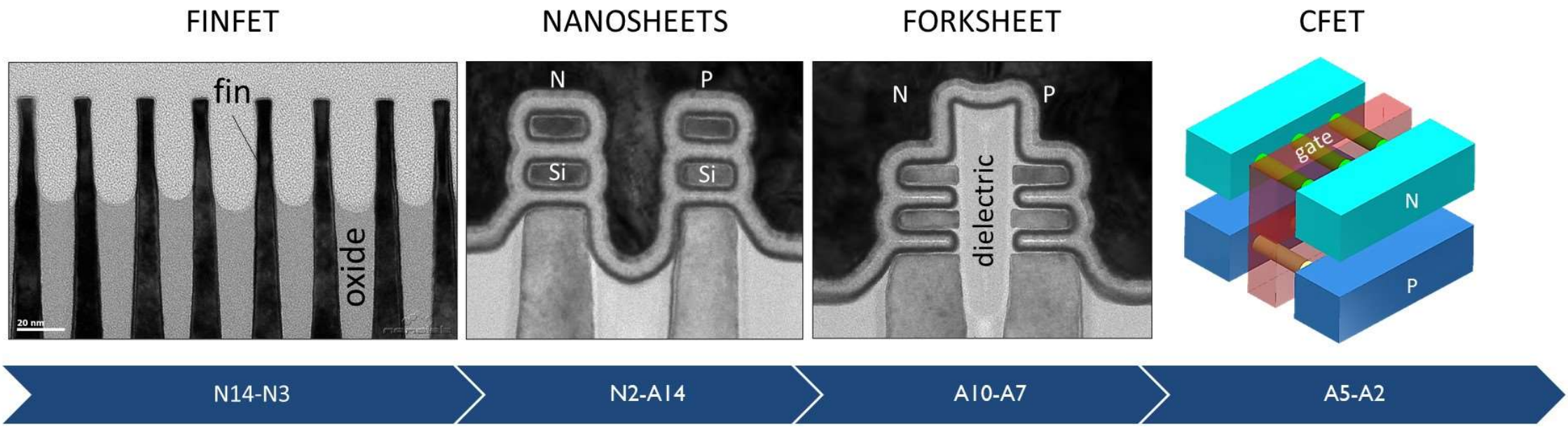
AR/VR

Low power
Ultra low latency
High memory bandwidth
Small form factor

Autonomous driving

Multi-sensor fusion
Distributed real-time computation
Reliable and explainable AI

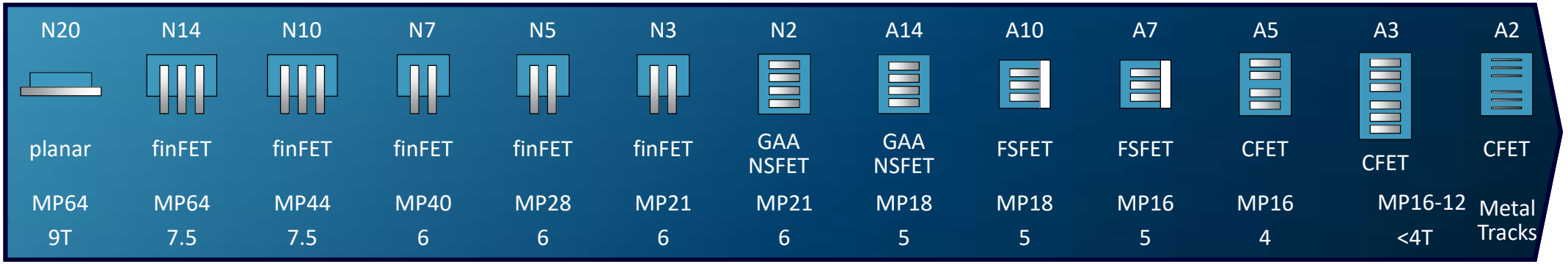
New device architectures to extend scaling

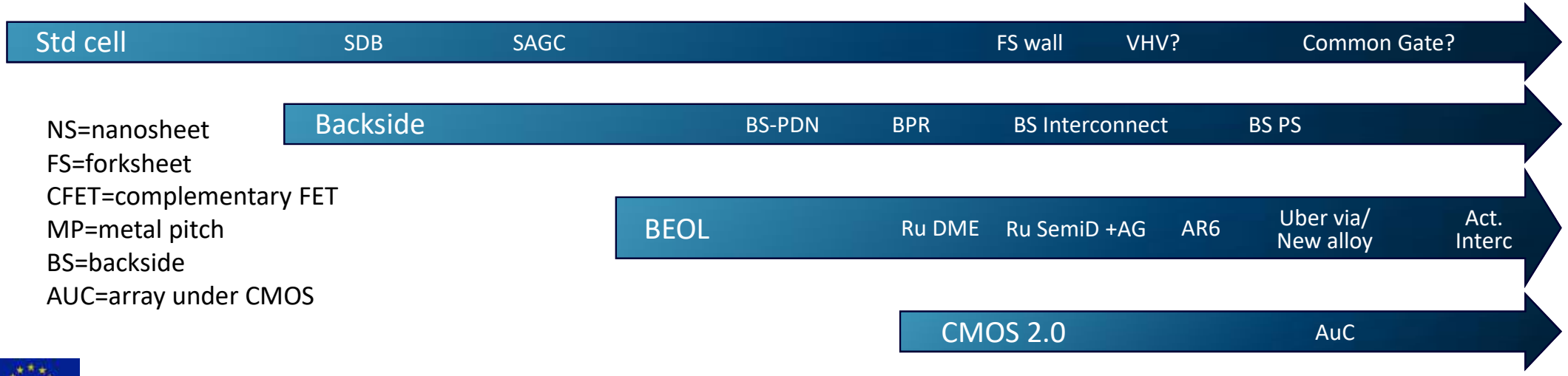


N. Collaert, "Advancements in IC Technologies: A look toward the future," in IEEE Solid-State Circuits Magazine, vol. 15, no. 3, pp. 80-86, 2023, doi: 10.1109/MSSC.2023.3280433.

Logic scaling roadmap

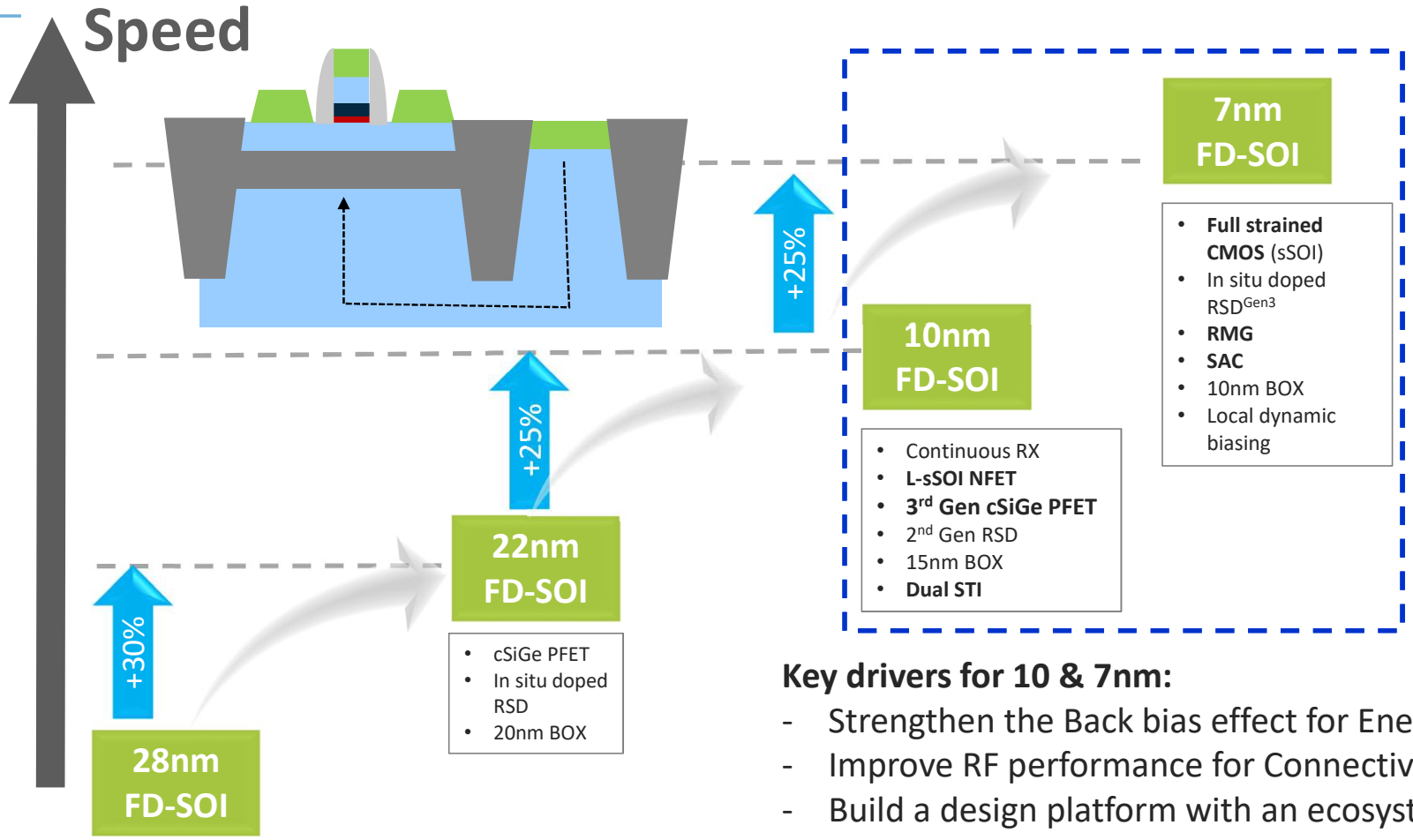
A. Veloso, ICOS workshop, April 2023.





NS=nanosheet
FS=forksheet
CFET=complementary FET
MP=metal pitch
BS=backside
AUC=array under CMOS

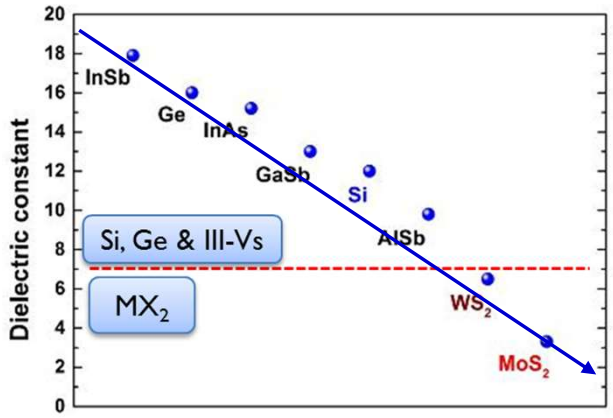
FD-SOI Technology Roadmap

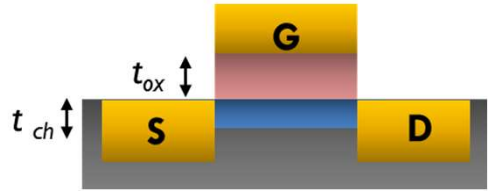


Key drivers for 10 & 7nm:

- Strengthen the Back bias effect for Energy saving
- Improve RF performance for Connectivity
- Build a design platform with an ecosystem

2D Channels: Next generation logic devices



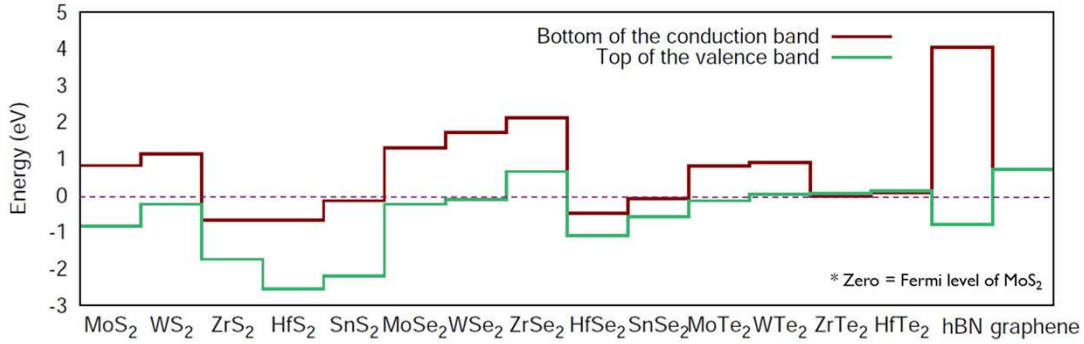


Characteristic length of short channel FETs:

$$\lambda = \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ch}.tox}$$

Expect reduced short channel effects in planar devices

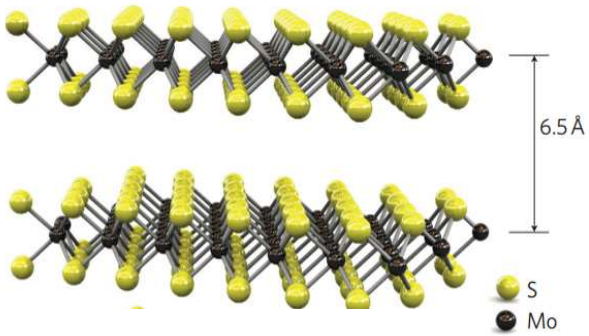
Ultra-thin materials



Choice of bandgaps and band alignment

No/few dangling bonds at interfaces

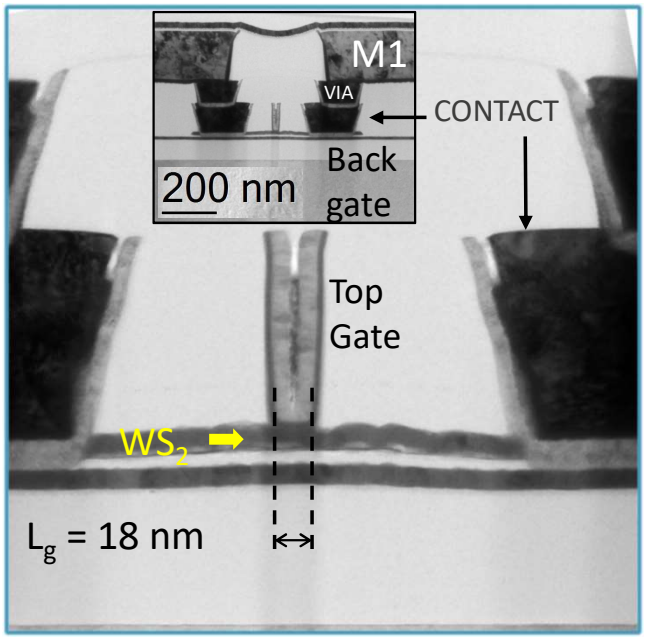
2D Channels: Next generation logic devices



MoS_2

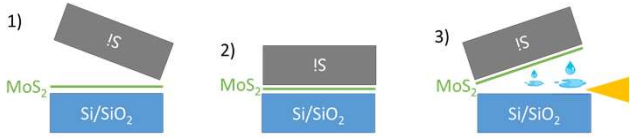
Monolayer channel thickness enables gate length scaling while keeping high performance

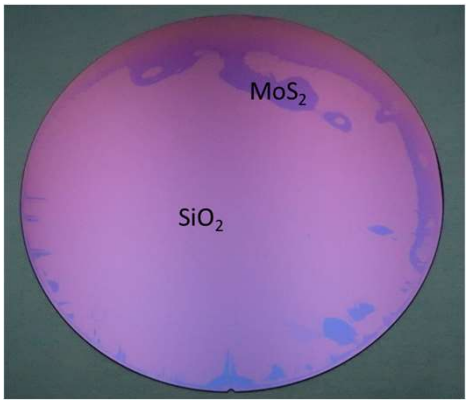
300mm Flow



I. Asselberghs et al, IEDM 2020

Layer Transfer





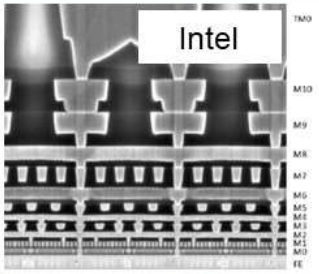
CEA-Leti, unpublished

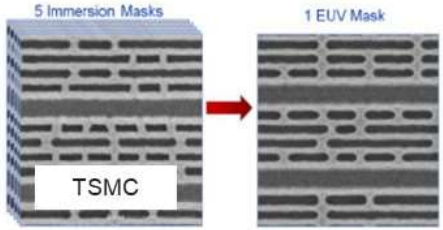
Industry BEOL trends

Courtesy: Zsolt Tokei (imec)

~36-40nm BEOL pitch

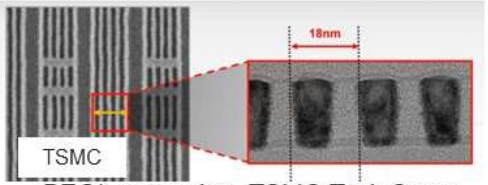
10nm technology, C. Auth et al. IEDM 2017





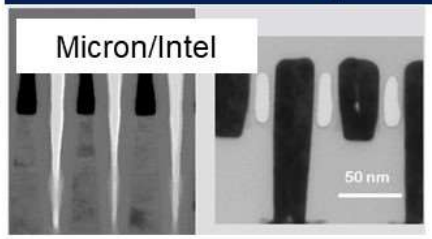
5nm CMOS, G. Yeap et al. IEDM2019

<20nm pitch

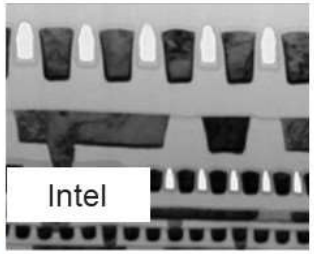


BEOL patterning, TSMC Tech Symp. 2020

AGs in memory & logic

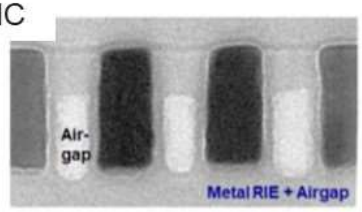


25nm NAND using air gaps K. Prall/K. Parat IEDM2010



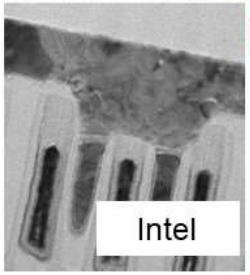
K. Fisher et al., 14nm, IITC2015

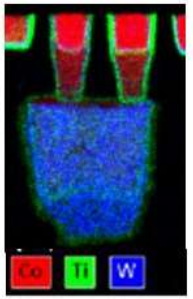
TSMC



Y.J. Mii et al. Keynote, VLS022

Co interconnects



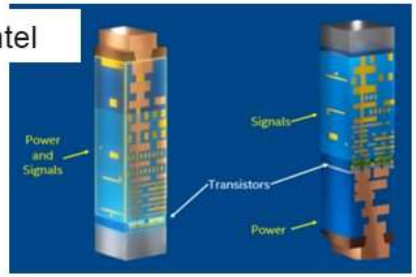


Self- aligned contact, C. Auth et al. IEDM 2017

Reliability of Co, F. Griggo et al. IRPS 2018

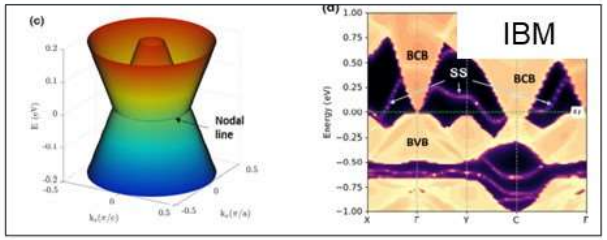
Backside Power Delivery

Intel

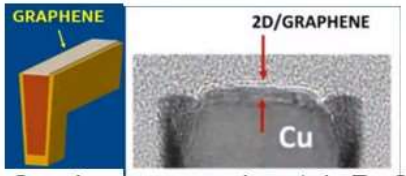


M.C. Mayberry, Keynote IITC 2020

New materials on the horizon

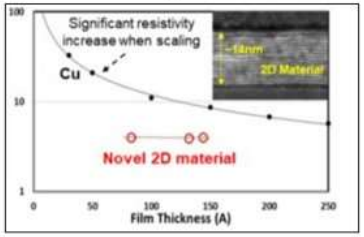


Topological semi-metal, C.T. Chen et al. IEDM2020



Intel

Graphene capped metal, R. Chau et al. Keynote IEDM2019

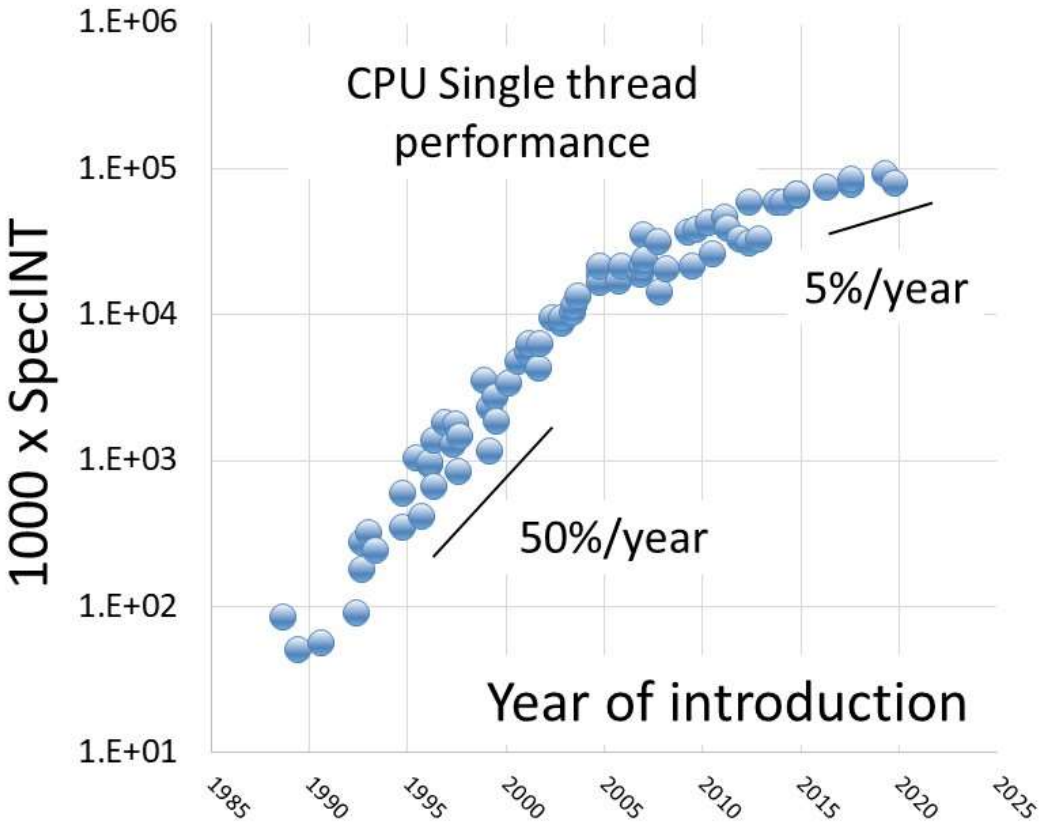


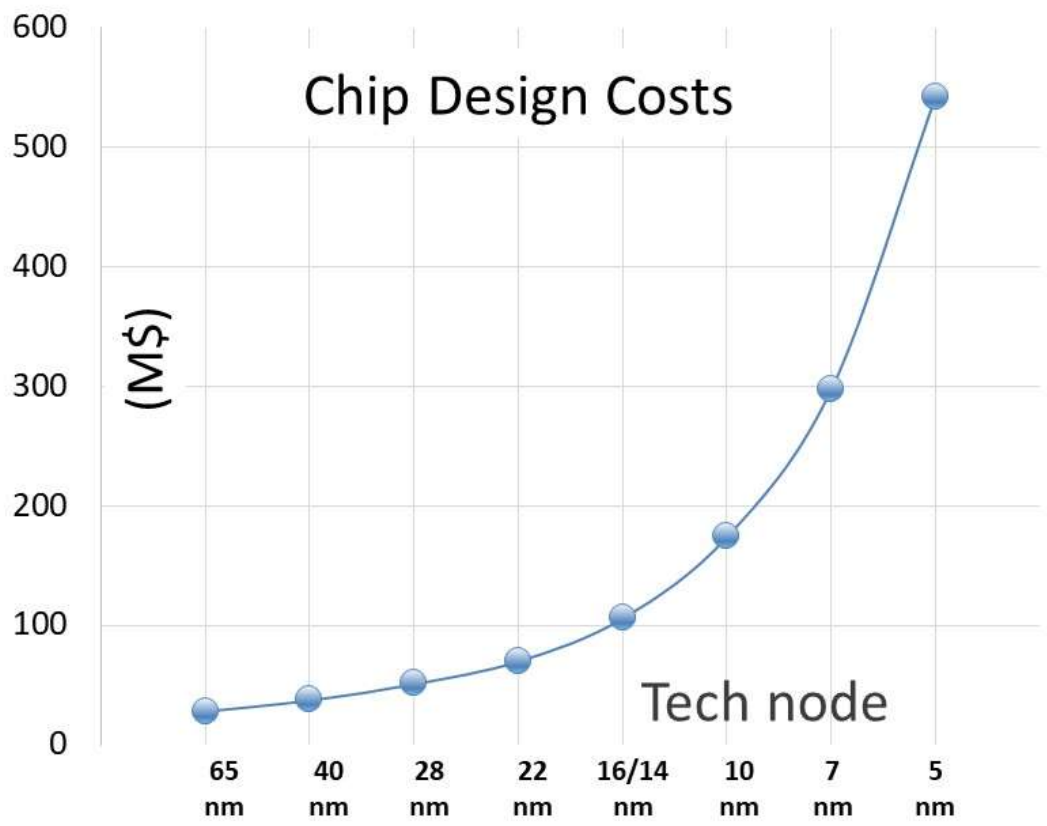
TSMC

New conductor, Y.J Mii Keynote VLSI2022

Pitch scaling, airgaps both in memory and logic, new materials

Slowdown in Performance and Increasing Costs

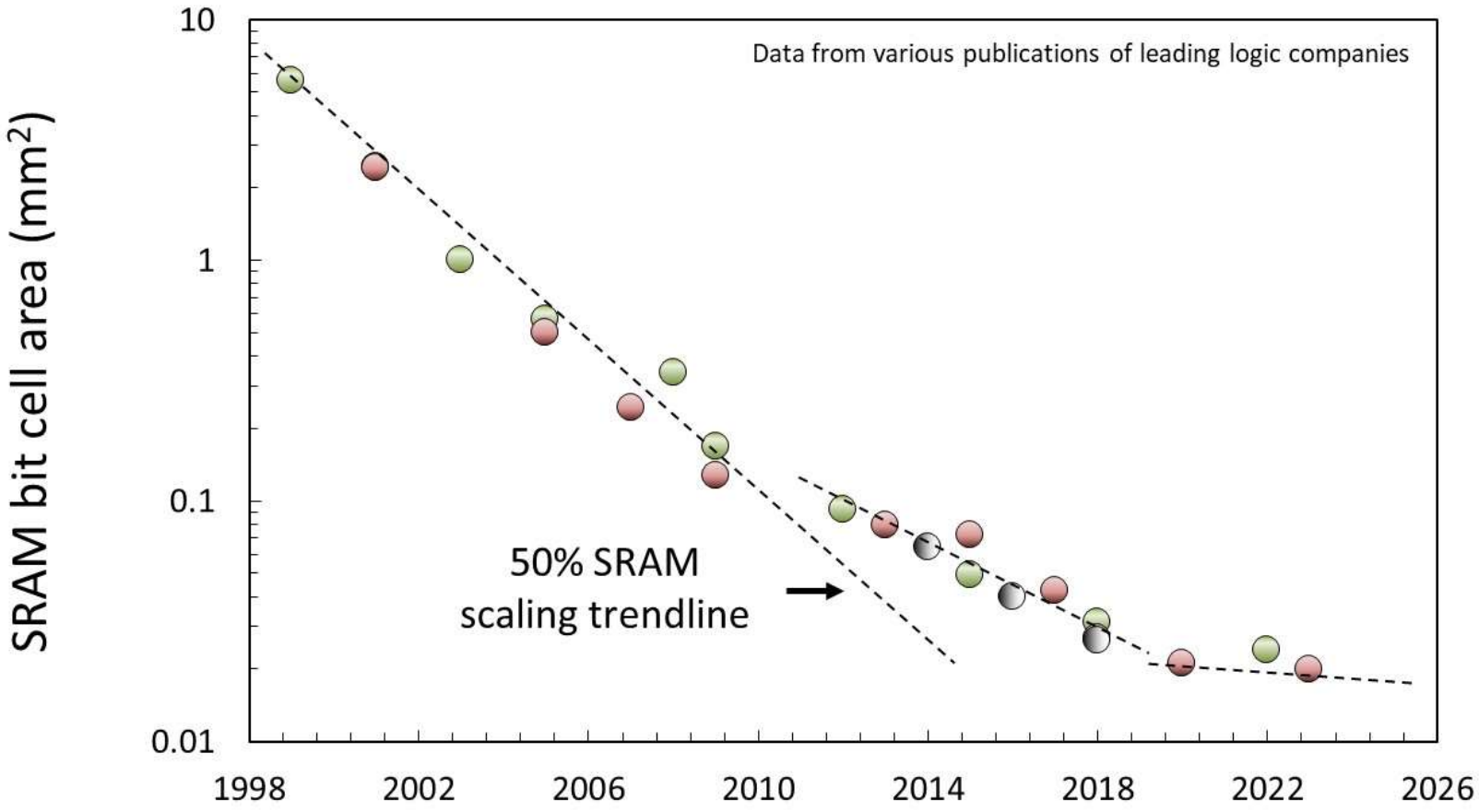




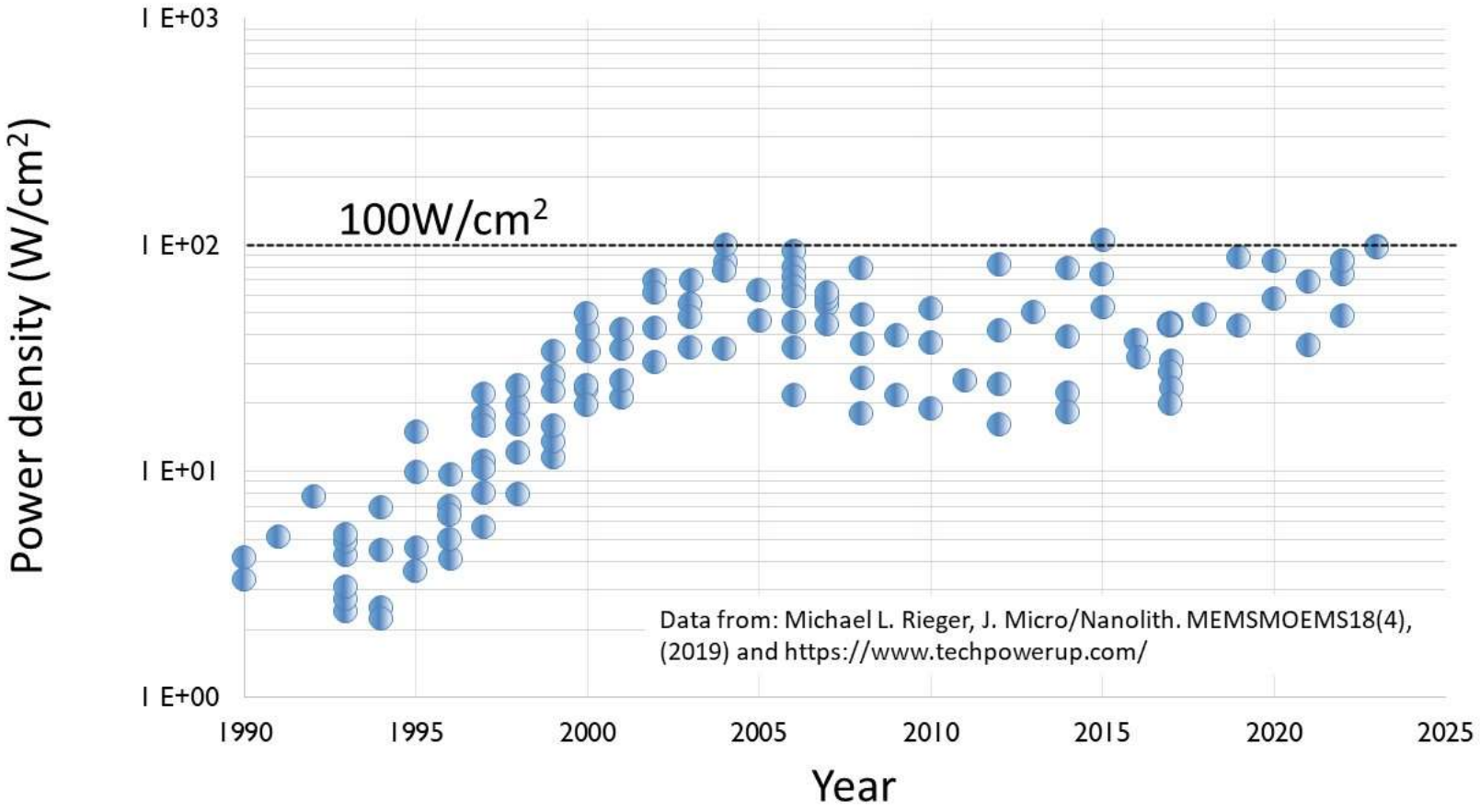
Based on original data plotted by M. Horowitz, F. Labonte, O. Shachan, K. Olukotun, L. Hammond, C. Batten. Additional data compiled by K. Rupp

Source: AI Chips and why they matter", S. Khan and A. Mann, 2020

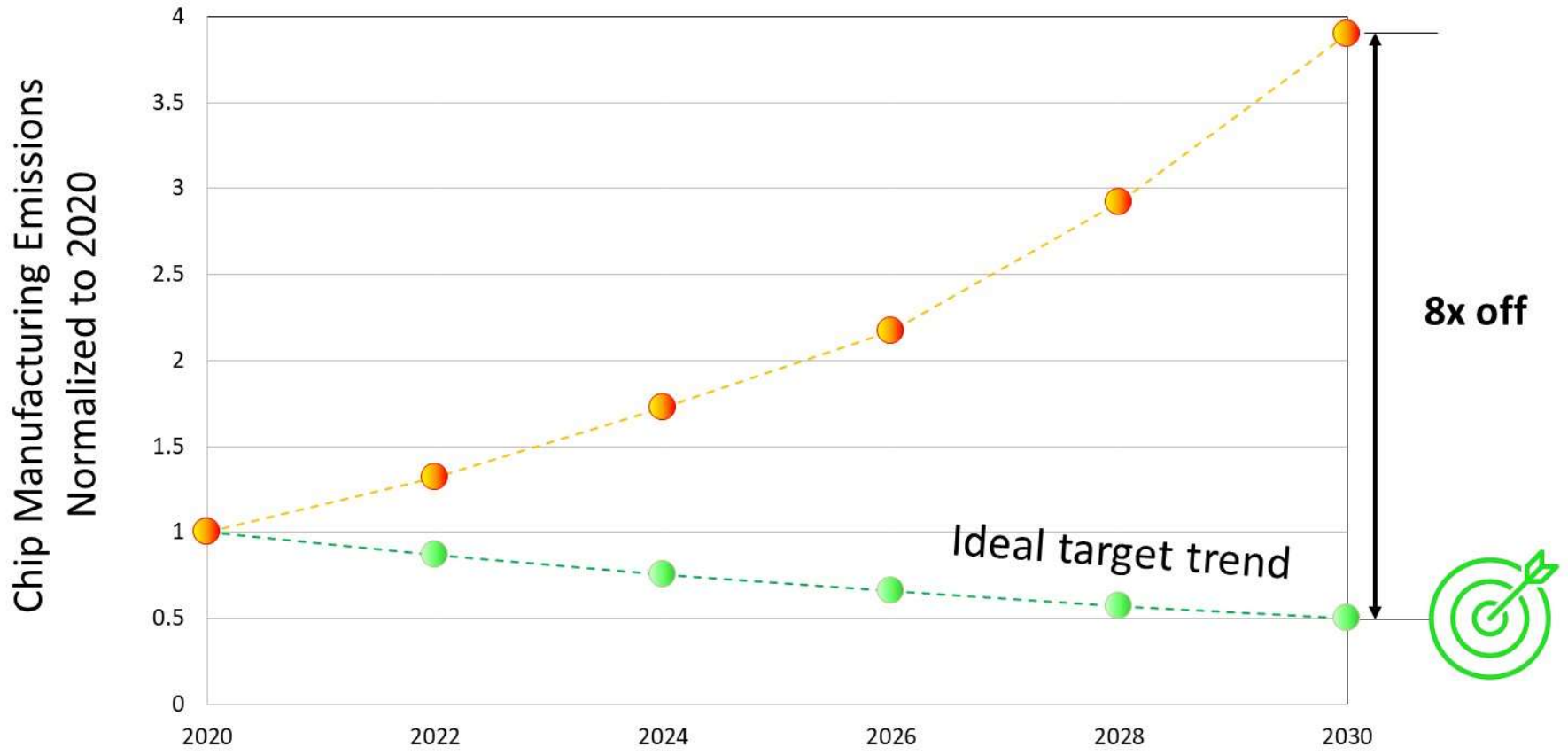
SRAM scaling has slowed down



Chip Cooling Limit Power Density of Chips

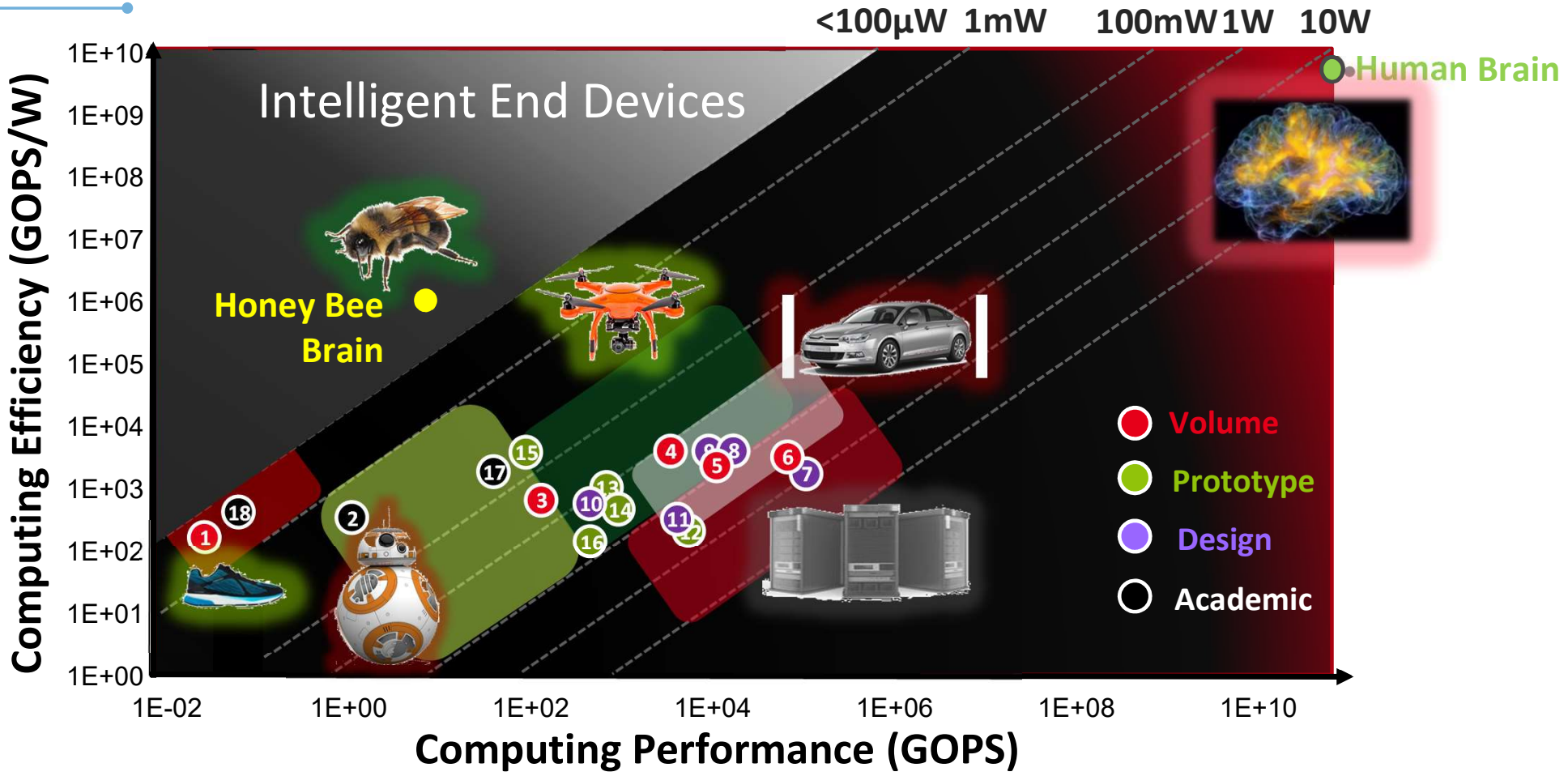


Carbon Emissions: “Do Nothing” Scenario

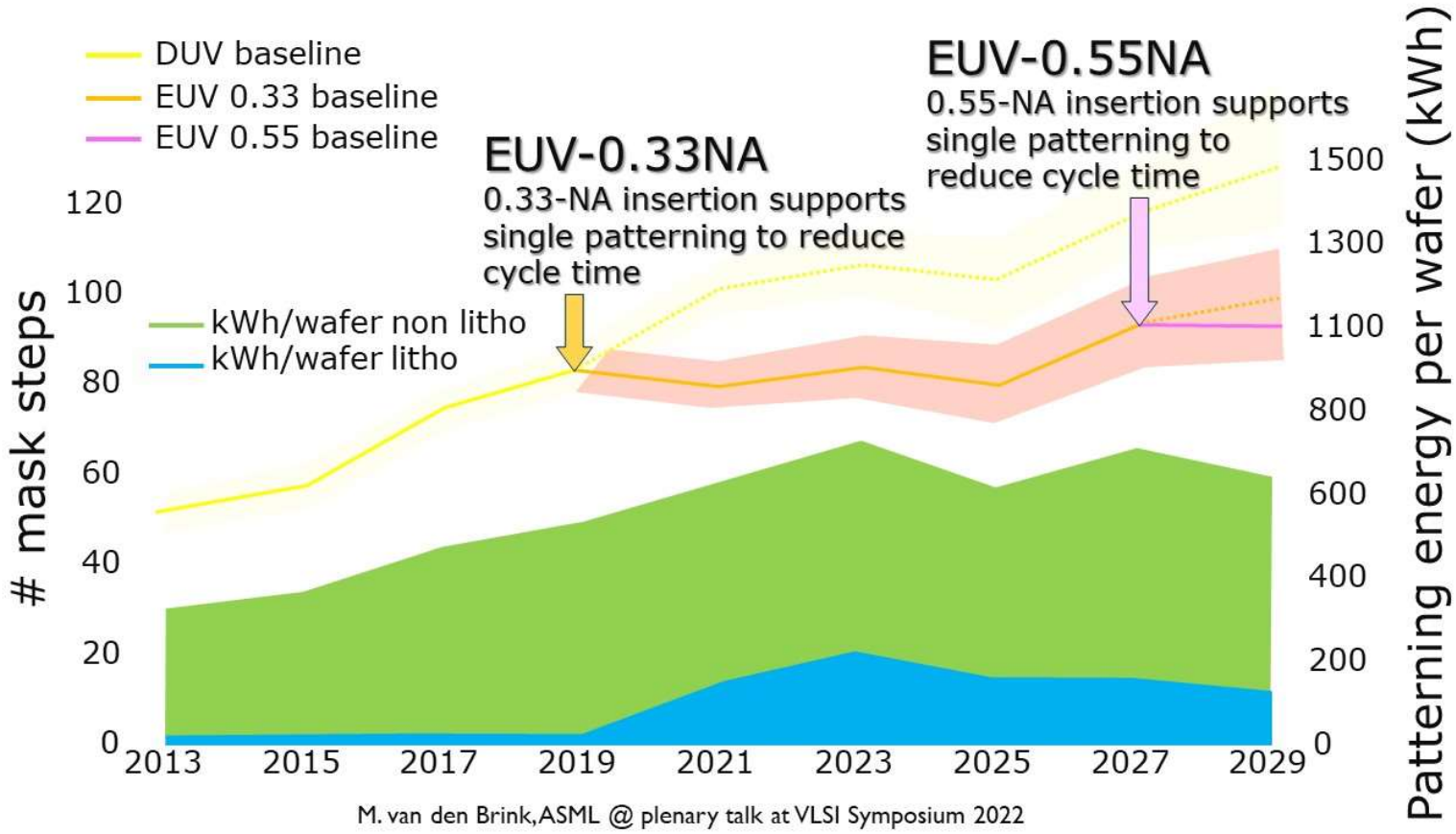


Constant electricity mix (0.49 kCO2eq/kWh), Abatement and GHG global warming potential according to IPCC assumed for the years 2020-2030. Volume technology mix from IBS “Foundry Market Trends and Strategic Implications” Vol 30, N 12 , Dec 2021. Logic nodes only. *imec.netzero emissions estimate of imec process nodes representative of foundry nodes.

Energy Efficiency is far from biological Systems



EUV lithography key enabler for scaling



Emerging Non-Volatile Memories

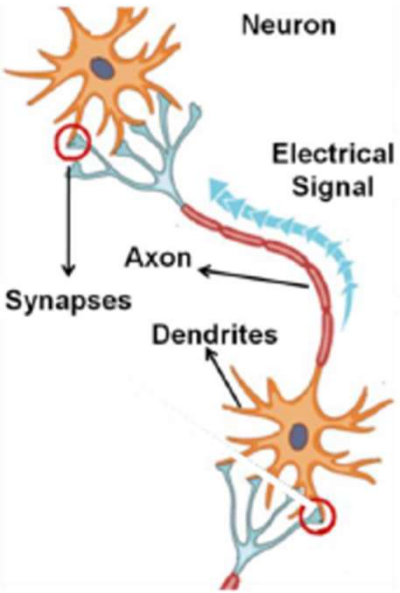
	NOR FLASH	MRAM	PCRAM	OxRAM	FeRAM (PZT)	FeRAM (HfO_2)
Programming power	~200pJ/bit	~20pJ/bit	~300pJ/bit	~100pJ/bit	**~10fJ/bit**	**~10fJ/bit**
Write speed	20 µs	**20 ns**	**10-100 ns**	**10-100 ns**	<100ns	**14ns @ 2.5V (SONY)** **4ns @ 4.8V (LETI)**
Endurance	10^5 - 10^6	**10^6-10^{15}**	10^8	10^5 – 10^6 on 16 kbit	**> 10^{15}**	**> 10^{11} single device** **10^6 – 10^7 on 16 kbit**
Retention	> 125°C	85°C - 165 °C	**165°C**	> 150°C	125°C	125°C
Extra masks	Very high (>10)	Limited (3-5)	Limited (3-5)	**Low (2)**	**Low (2)**	**Low (2)**
Process flow	Complex	Medium	Medium	**Simple**	**Simple**	**Simple**
Multi-Level Cell	Yes	No	**Yes**	**Yes**	No	No
Scalability	Bad	Medium	**High**	**High**	Medium	**Poor (2D)** **High (3D)**

Power Reduction by 10000!

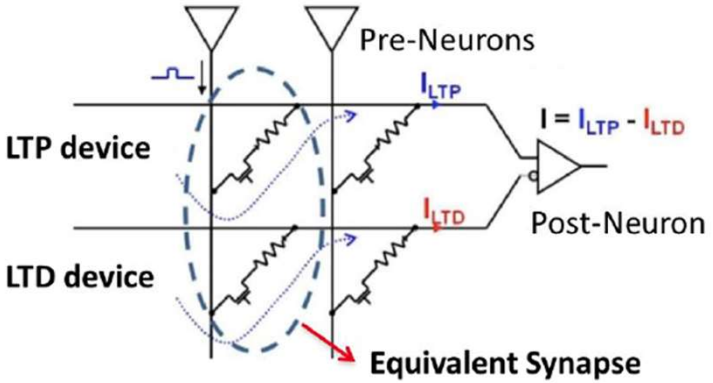
Memory activity focus on embedded NVM for NOR flash replacement

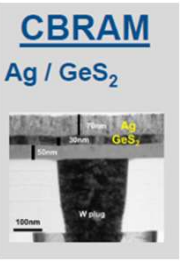
Neuromorphic based RRAM circuit

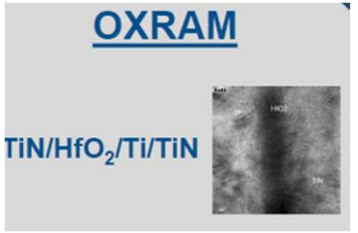
M. Suri et al, IEDM 2011.



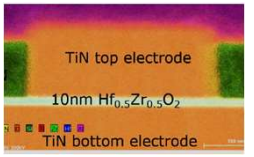
2 PCRAM Example:



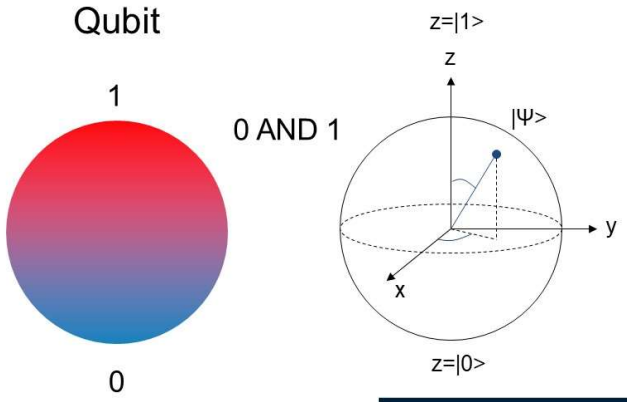




FeRAM

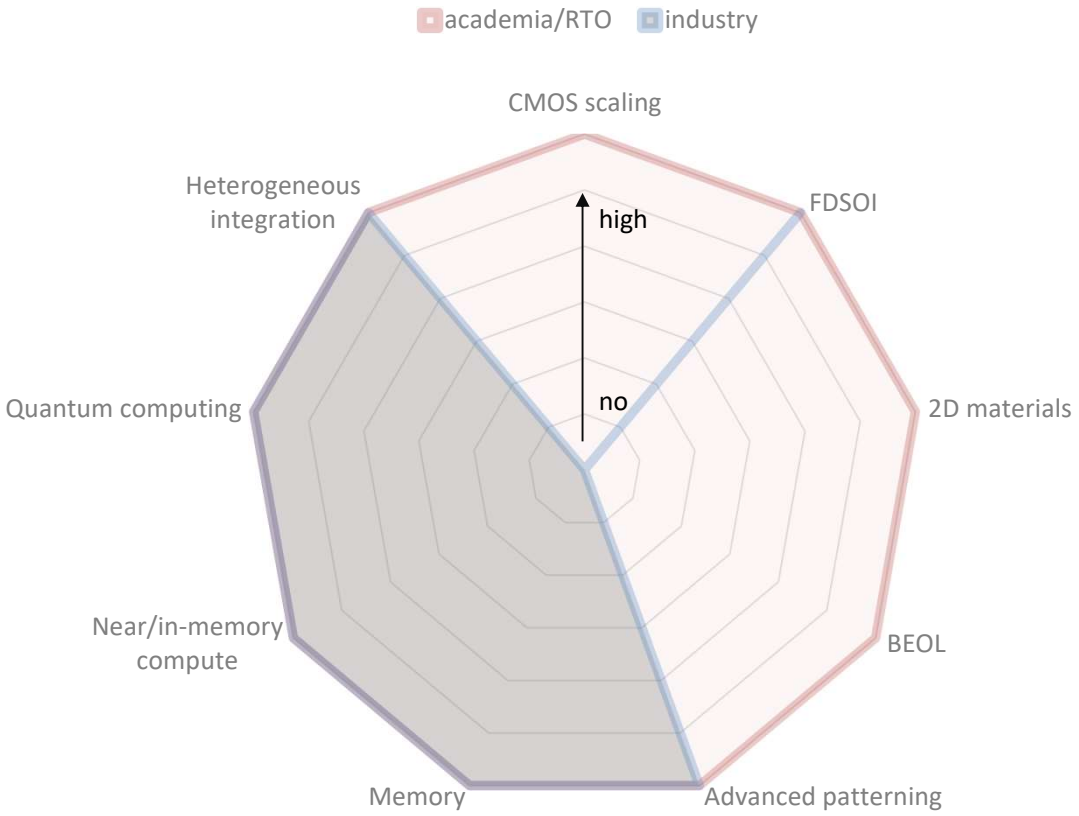


From bits to qubits



	Superconductor	Si spin qubit	Trapped ion	Photon
Size*	(100μm)²	(100nm)²	(1mm)²	~(100μm)²
1qubit fidelity	99.96%	99.93%	99.98%	
2qubit fidelity	~99.3%	>99%	99.9%	50% (measurement) 98% (gates)
Speed**	12-400 ns	~1 μs	100 μs	1 ms
Variability	3%	0.1%-0.5%	0.01%	0.5%
T° of operation	15mK	1K	10K	4K/10K
Entangled qubits	433 (IBM)	3 (TU) (6 - QuTech)	32 (IonQ)	70 (Pan-China)

EU and non-EU actors - EU



- R&D very strong in all areas of compute
- Unique strong position in EUV lithography
- In general, industrial EU players lacking to take up R&D

Challenges in Advanced Computing and Functionalities International Cooperation on Semiconductors

Thank you for your attention

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